

**Low-Noise Phase-Locked Loop
Clock Driver with 9 Clock Outputs**

Product Features

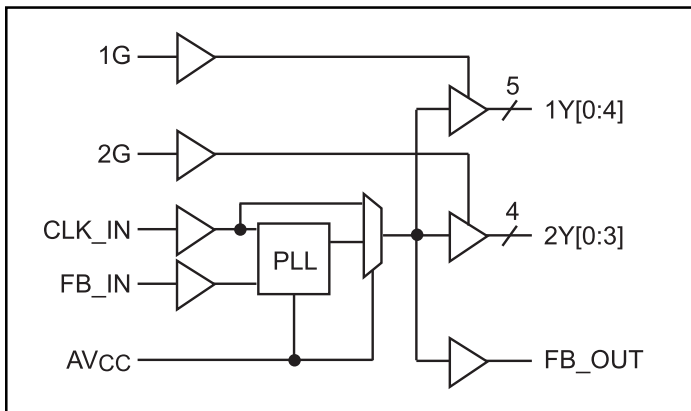
- Operating Frequency up to 150 MHz
- Low-Noise Phase-Locked Loop Clock Distribution to meet 133 MHz Registered DIMM Synchronous DRAM module specifications for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-output delay: Distribute One Clock Input to one bank of five and one bank of four outputs, with separate output enables
- Low jitter: Cycle-to-Cycle jitter ± 75 ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Package: Plastic 24-pin TSSOP (L)

Product Description

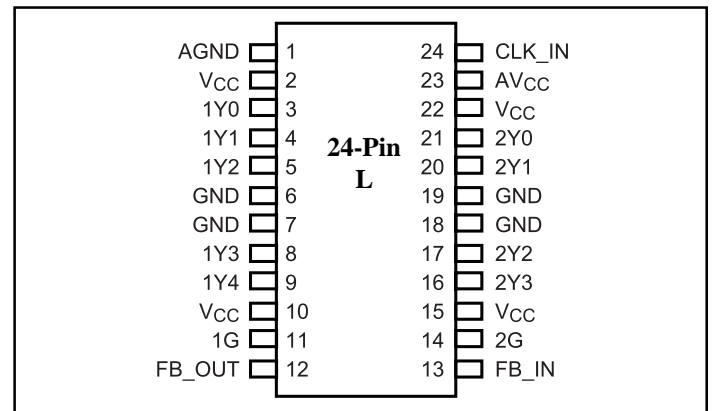
The PI6C2509-133 is a “quiet,” low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing low-noise clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK_IN input clock to be distributed, providing 5 clocks for the first bank, and an additional 4 clocks for the second bank.

This clock driver is designed to meet the PC133 SDRAM Registered DIMM specification. For test purposes, the PLL can be bypassed by strapping AV_{CC} to ground.

Logic Block Diagram



Product Pin Configuration



Functional Table

Input Control	Outputs	
X ⁽¹⁾ G	X ⁽¹⁾ Y[0:3]	FB_OUT
L	L	CLK_IN
H	CLK_IN	CLK_IN

Note:

1. X is either 1 or 2

Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	24	I	Clock input. CLK_IN allows spread spectrum.
FB_IN	13	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
1G	11	I	Output bank enable. When 1G is LOW, outputs 1Y[0:4] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:4] are enabled.
2G	14	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled.
FB_OUT	12	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Yx, 2Yx.
1Y[0:4]	3,4,5,8,9	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
2Y[3:0]	16,17,20,21	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AVCC	23	Power	Analog power supply. AVCC can be also used to bypass the PLL for test purposes. When AVCC is strapped to ground, PLL is bypassed and CLK_IN. is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VCC	2,10,15,22	Power	Power supply.
GND	6,7,18,19	Ground	Ground.

DC Specifications

Absolute maximum ratings over operating free-air temperature range.

Symbol	Parameter	Min.	Max.	Units
V _I	Input voltage range	-0.5	V _{CC} + 0.5	V
V _O	Output voltage range			
V _{I_DC}	DC input voltage		+5.0	
I _{O_DC}	DC output current		100	mA
Power	Maximum power dissipation at T _A = 55°C in still air		1.0	W
T _{STG}	Storage temperature	-65	150	°C

Note:

Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	V _{CC}	Min.	Typ.	Max.	Units
I _{CC}	V _I = V _{CC} or GND; I _O = 0 ⁽¹⁾	3.6V			10	μA
C _I	V _I = V _{CC} or GND	3.3V		4		pF
C _O	V _O = V _{CC} or GND			6		

Note:

1. Continuous output current

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply voltage	3.0	3.6	V
V _{IH}	High level input voltage	2.0		
V _{IL}	Low level input voltage		0.8	
V _I	Input voltage	0.0	V _{CC}	
T _A	Operating free-air temperature	0	70	°C

Electrical characteristics over recommended operating free-air temperature range

Pull Up/Down Currents of PI6C2509-133, V_{CC} = 3.0V

Symbol	Parameter	Condition	Min.	Max.	Units
I _{OH}	Pull-up current	V _{OUT} = 2.4V		-13.6	mA
	Pull-up current	V _{OUT} = 2.0V		-22	
I _{OL}	Pull-down current	V _{OUT} = 0.8V	19		
	Pull-down current	V _{OUT} = 0.55V	13		

AC Specifications

Timing requirements over recommended ranges of supply voltage and operating free-air temperature.

Symbol	Parameter	Min.	Max.	Units
F _{CLK}	Input clock frequency	25	150	MHz
	Input clock duty cycle	40	60	%
	Stabilization time after power up		1	ms

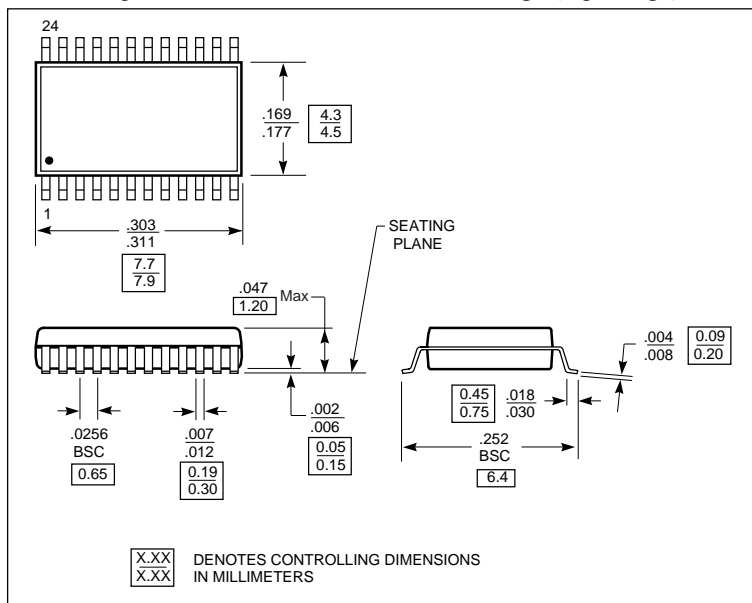
Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L=30pF

Parameter	From	To	V _{CC} = 3.3V ±0.3V, 0-70°C			Units
			Min.	Typ.	Max.	
t _{phase error} , with and without Spread Spectrum	CLK_IN↑ at 133 MHz	FB_IN↑	-150		+150	ps
Jitter, cycle-to-cycle with and without Spread Spectrum	Any Output or FB_OUT in CLK _n at 133 MHz	Output or FB_OUT in CLK _{n+1}	-75		+75	
Skew, at 133 MHz	Any Y or FB_OUT				150	
Duty cycle		Any Y or FB_OUT	45	50	55	%
t _r , rise-time, 0.4V to 2.0V				1.0		ns
t _f , fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed, but not production tested.

Package Mechanical Information

Plastic 24-pin Thin Shrink Small-Outline Package (L package).



Ordering Information

Part Number	Operating Frequency Range	Ordering P/N
PI6C2509-133	25 MHz - 150 MHz	PI6C2509-133L